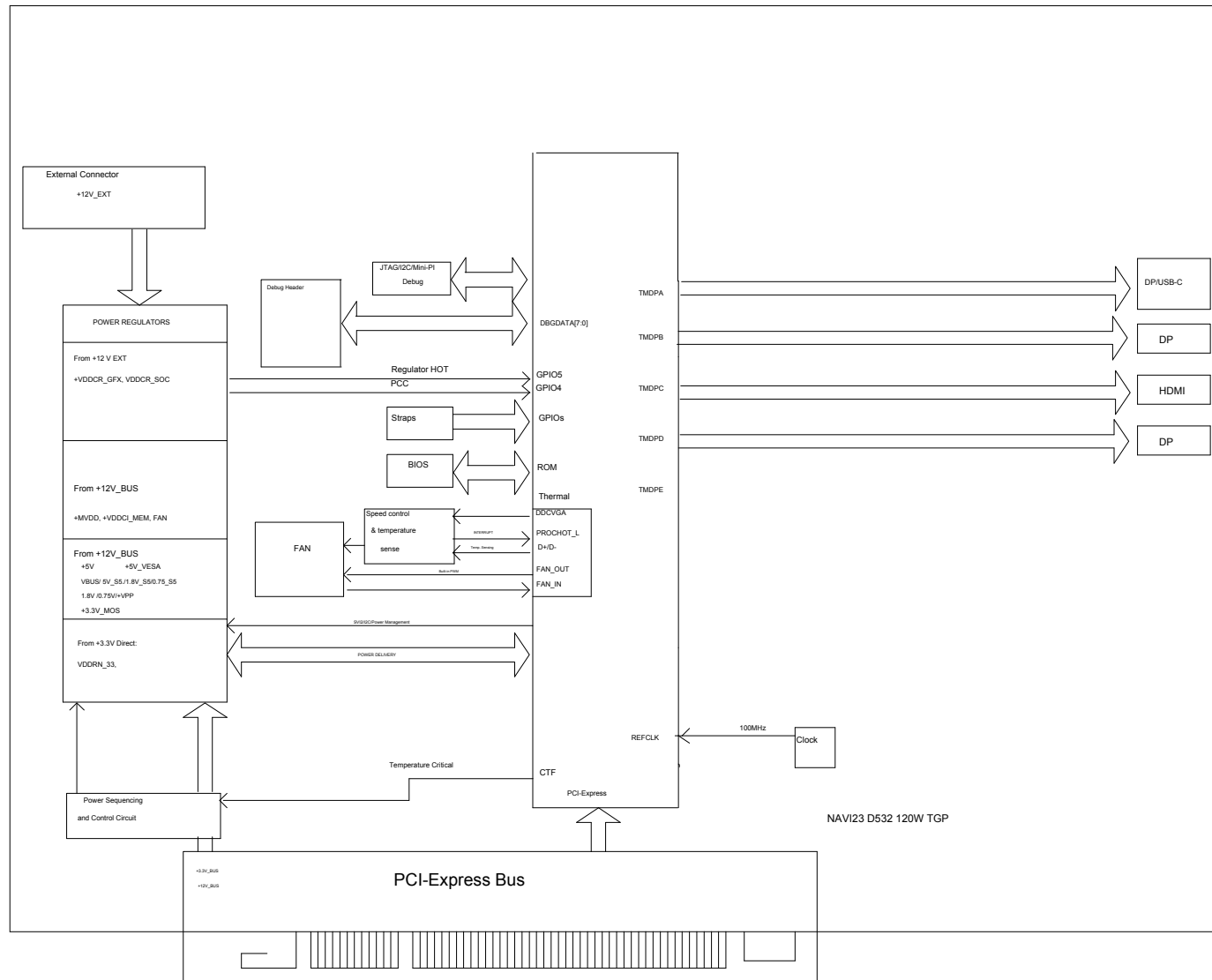


NAVI23 GDDR6 4PCS,8L DP/USB-C + DP + HDMI + DP

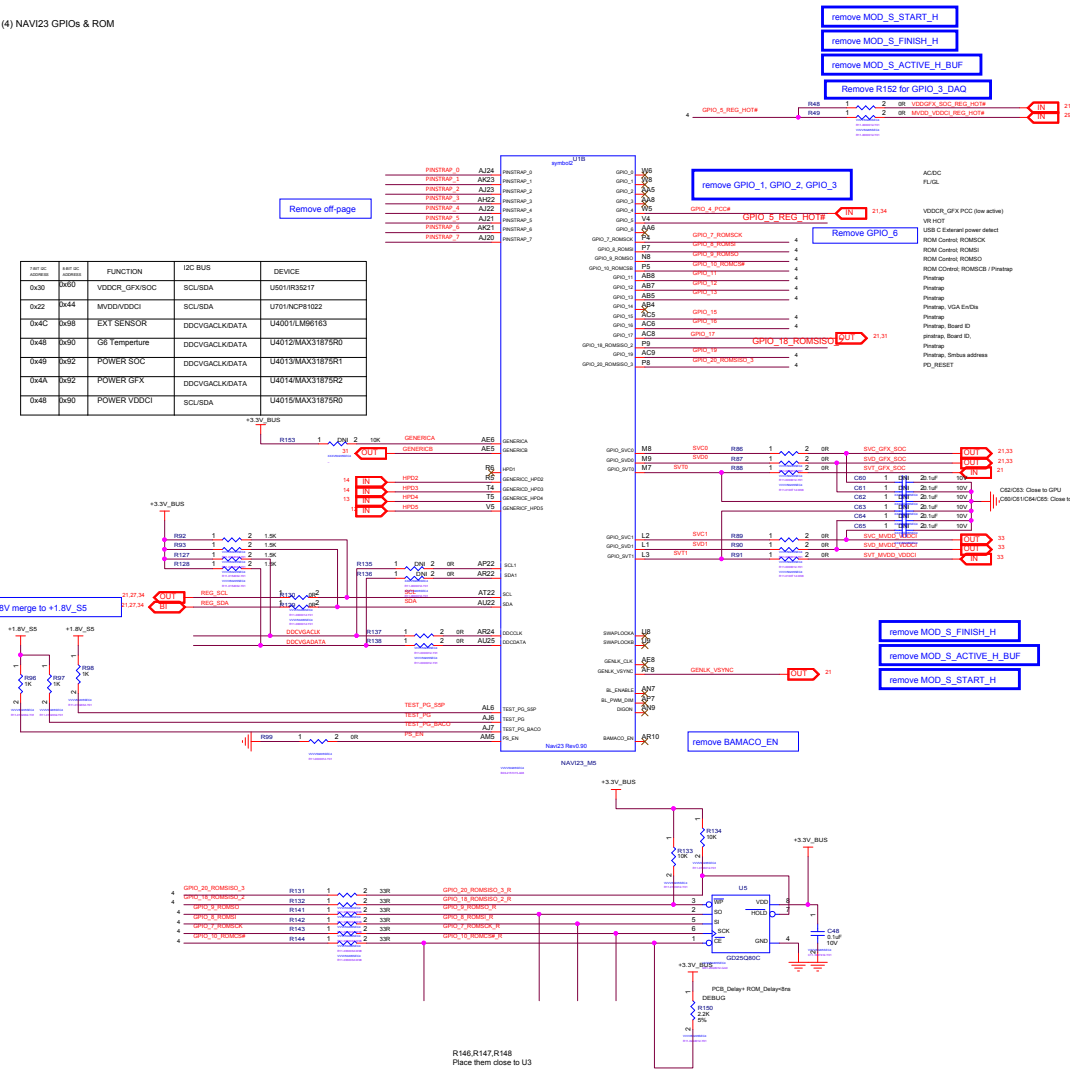
105-D532xx-00 Rev00B Desktop board(120W TGP)

TABLE OF CONTENTS

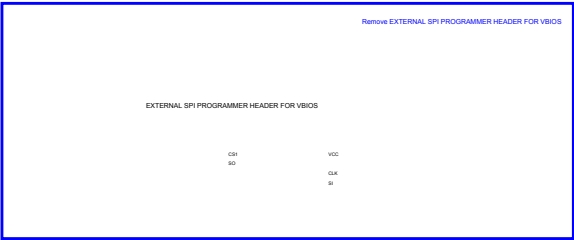
SHEET NO.	SHEET NAME	SHEET NO.	SHEET NAME
1	TOC	26	REG 5V
2	BLOCK DIAGRAM	27	MVDD_VDDCI CONTROLLER
3	NAVI23 - PCIe Interface	28	REG MVDD
4	NAVI23- GPIO, EXTRA	29	REG VDDCI
5	NAVI23 - XTAL	30	SMALL RAIL LDO
6	NAVI23 - POWER and GND	31	MECHANICAL AND THERMAL
7	NAVI23 - Decaps	32	POWER MANAGEMENT
8	NAVI23 - MEM CH AB	33	SVI2
9	NAVI23 - MEM CH CD	34	DEBUG CIRCUITS
10	GDDR6 x16 - MEM CH AB	35	MINI PI
11	GDDR6 x16 - MEM CH CD	36	REVISION HISTORY
12	NAVI23 - TMDPA - USB/DP		
13	NAVI23 - TMDPB - DP		
14	NAVI23 - TMDPCD- HDMI,DP		
15	PD CONTROLLER		
16	USB-C PORT 1& DP		
17	3.3V_AUX		
18	USB_VBUS 5V S5_Rails		
19	REG 1.8V 0.75V VPP		
20	MODS CONTROL & POWER		
21	GFX & SOC CONTROLLER		
22	VDDCR_GFX PHASES 2 and 5		
23	VDDCR_GFX PHASES 1 and 4		
24	VDDCR_GFX PHASES 3 and 6		
25	VDDCR_SOC		





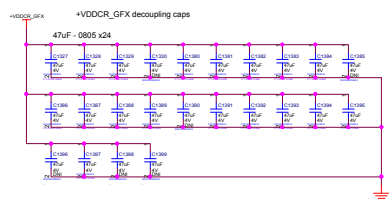
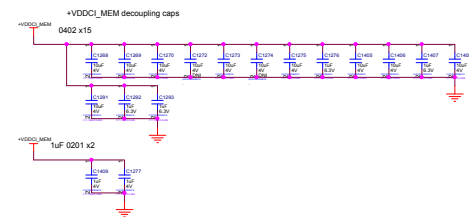
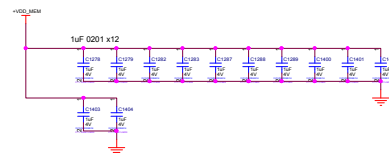
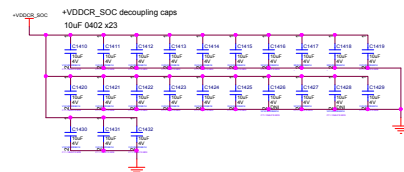
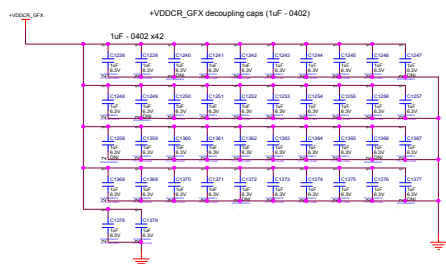


		Internal Default Value		Definition	
User	BIF	R01	1 2 10K	PINSTRAP_5	4
		R02	1 2 10K	PINSTRAP_7	4
		R03	1 2 10K	GPIO_13	4
		R04	1 2 10K	GPIO_15	4
DCE	DCE	R05	1 2 10K	PINSTRAP_3	4
		R06	1 2 10K	PINSTRAP_4	4
		R07	1 2 10K	GPIO_12	4
		R08	1 2 10K	GPIO_11	4
Platform	Platform	R09	1 2 10K	GPIO_14_ROM/SSIO_2	4
		R10	1 2 10K	GPIO_17	4
		R11	1 2 10K	GPIO_16	4
		R12	1 2 10K	GPIO_18	4
SMU	SMU	R13	1 2 10K	PINSTRAP_2	4
		R14	1 2 10K	PINSTRAP_1	4
		R15	1 2 10K	PINSTRAP_3	4
		R16	1 2 10K	GPIO_19	4

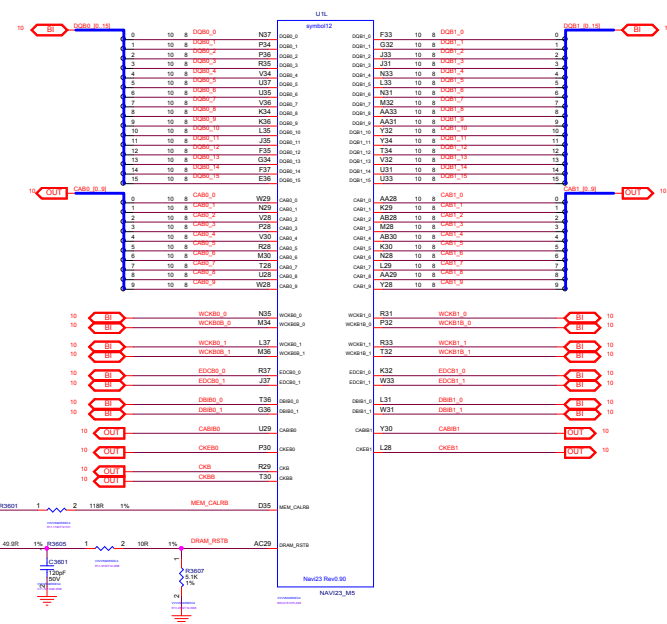
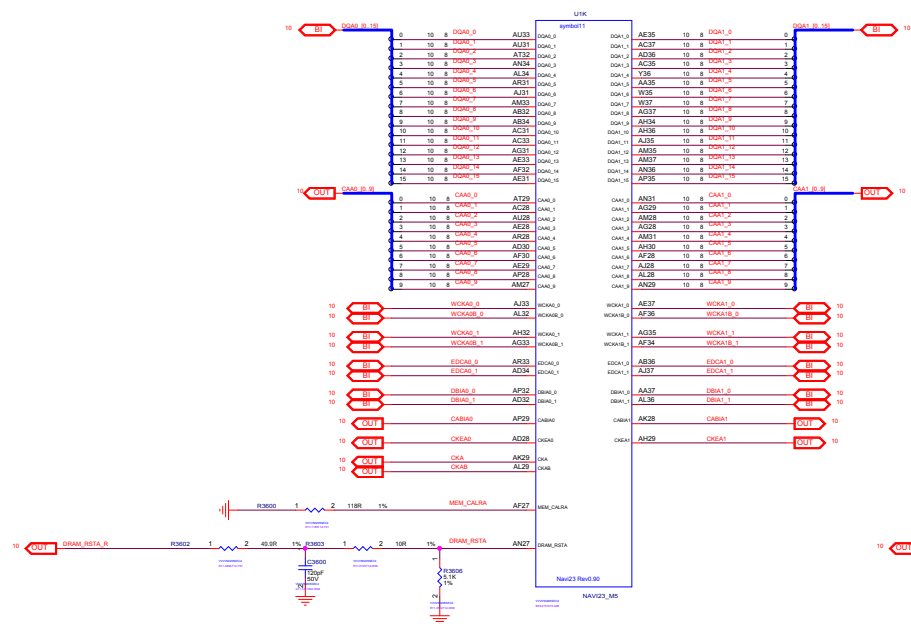






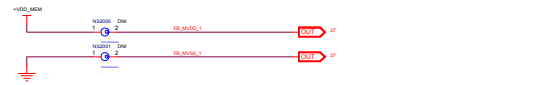
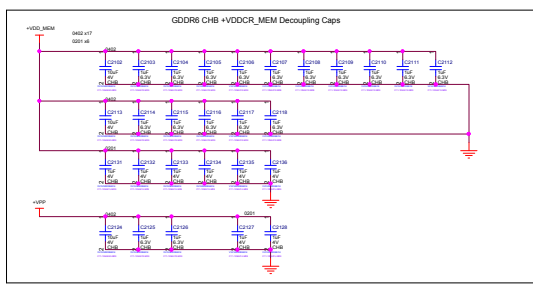
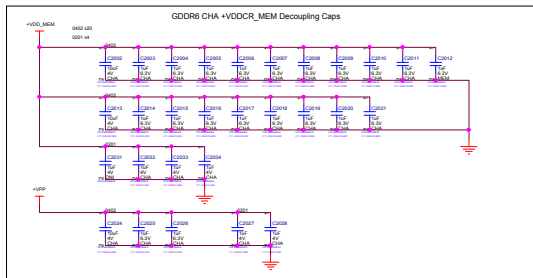
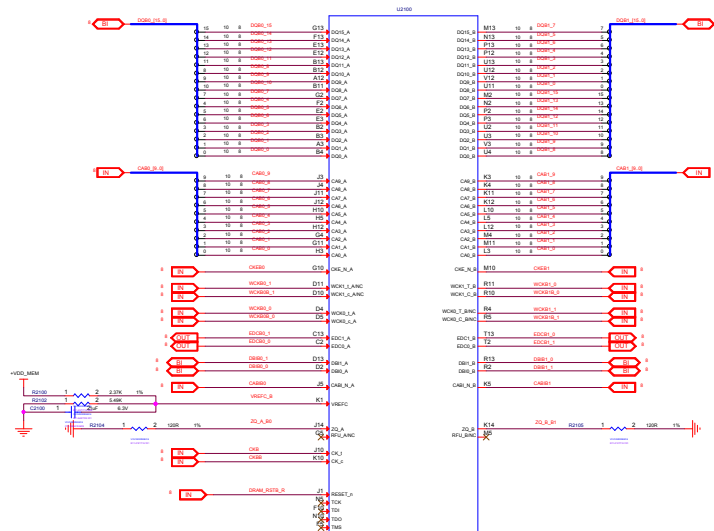
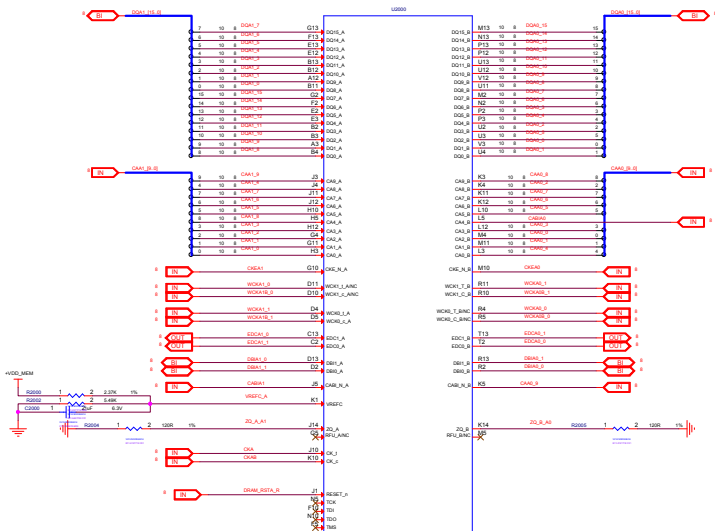


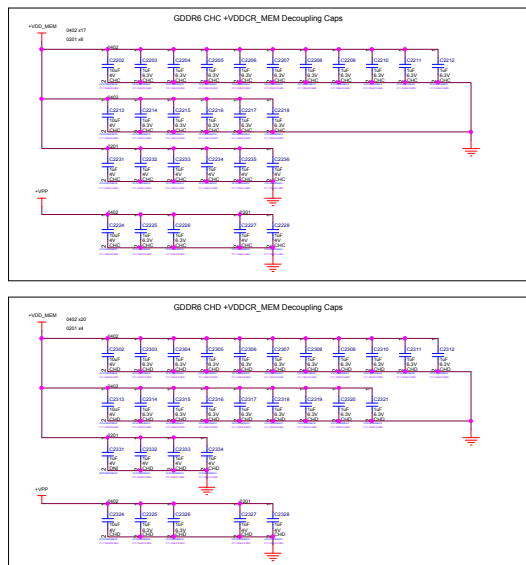
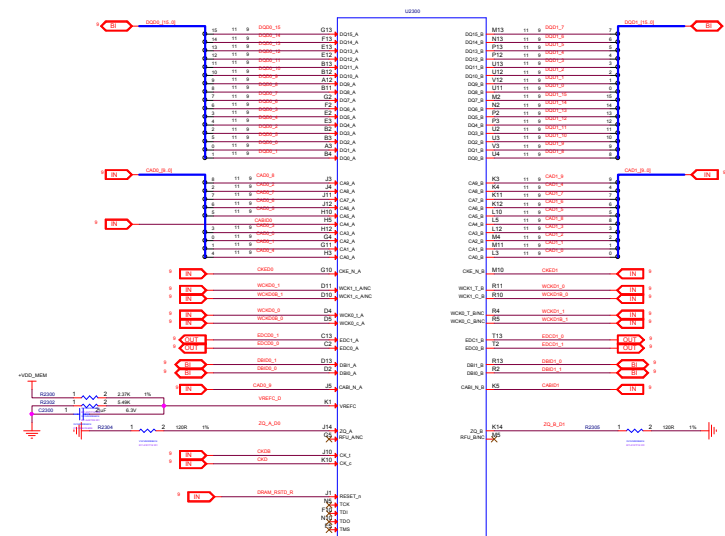
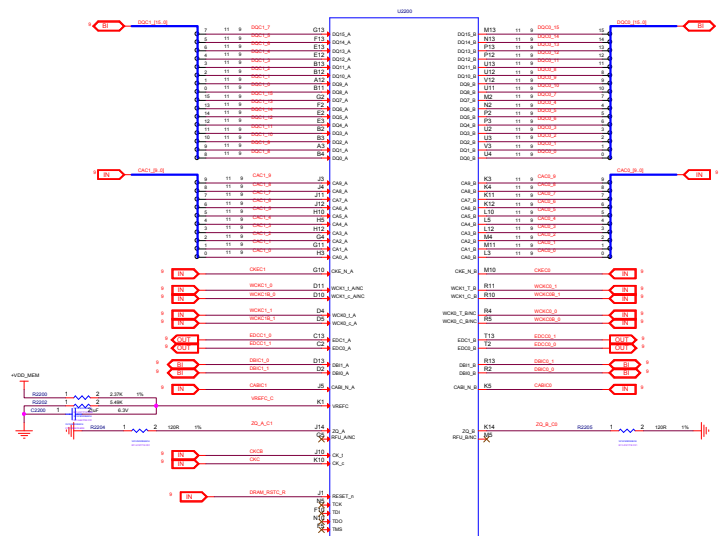
## (8) NAVI23 MEM INTERFACE CH A/B



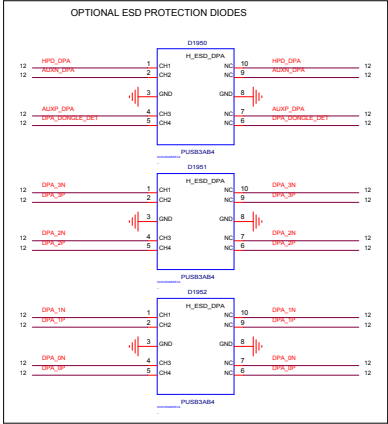
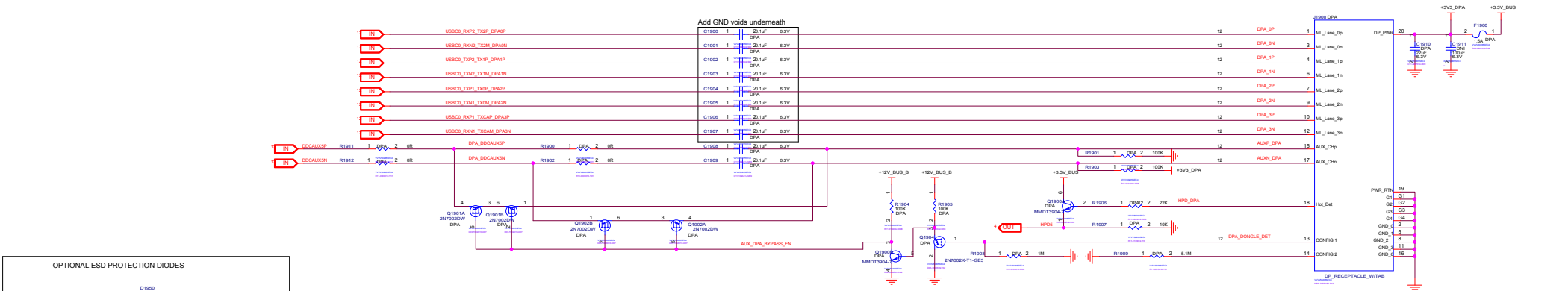
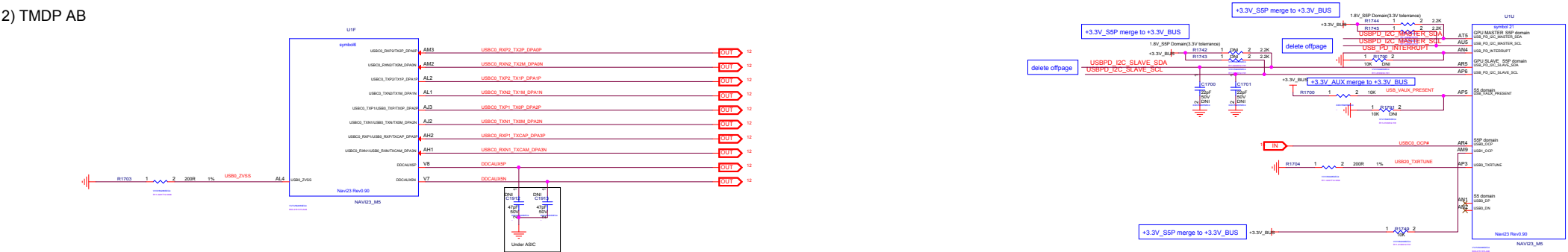


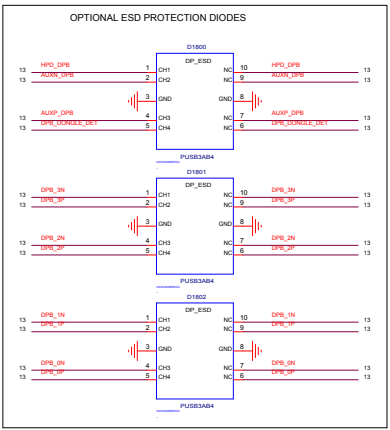


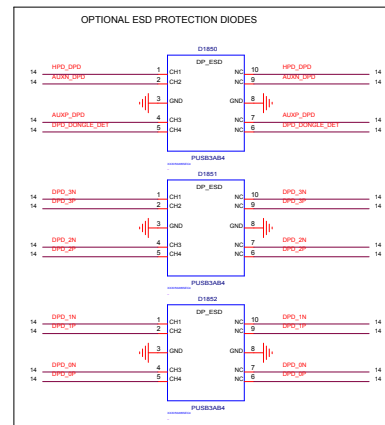
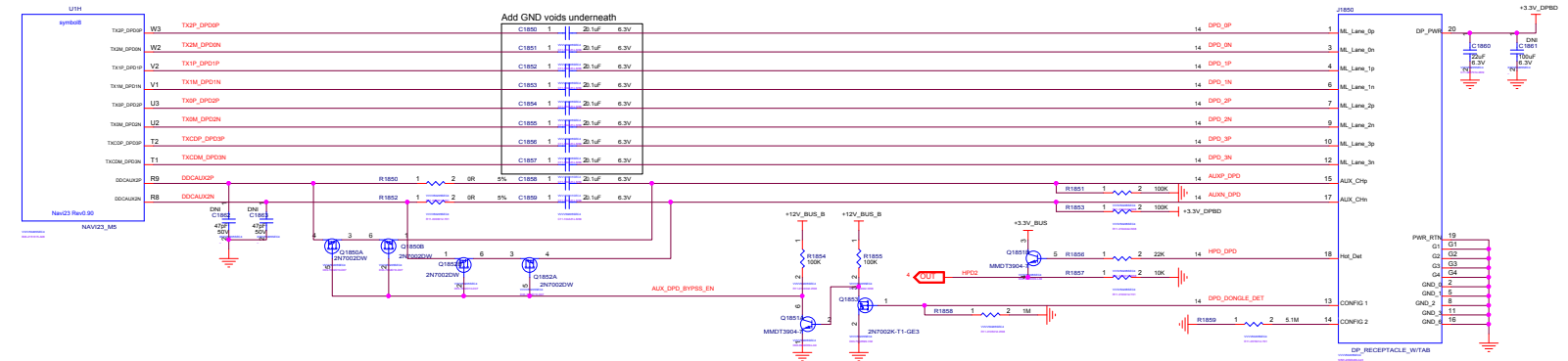


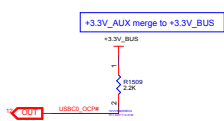


(12) TMDP AB









remove

Remove



remove



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MS-V502

Size	Document Description	Rev
Custom	0017 3.3V_AUX	2.0
Date: Wednesday, May 19, 2021		Sheet 17 of 37

+3.3V\_12V merge to +3.3V\_BUS

remove

+0.75V merge to +0.75V\_SS

+1.8V merge to +1.8V\_SS



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MS-V502

Size	Document Description	Rev
Custom	0016 USB_VBUS SV SS_Rails	2.0
Date: Wednesday, May 15, 2024		Sheet 18 of 37



remove

remove +5V\_S5 offpage

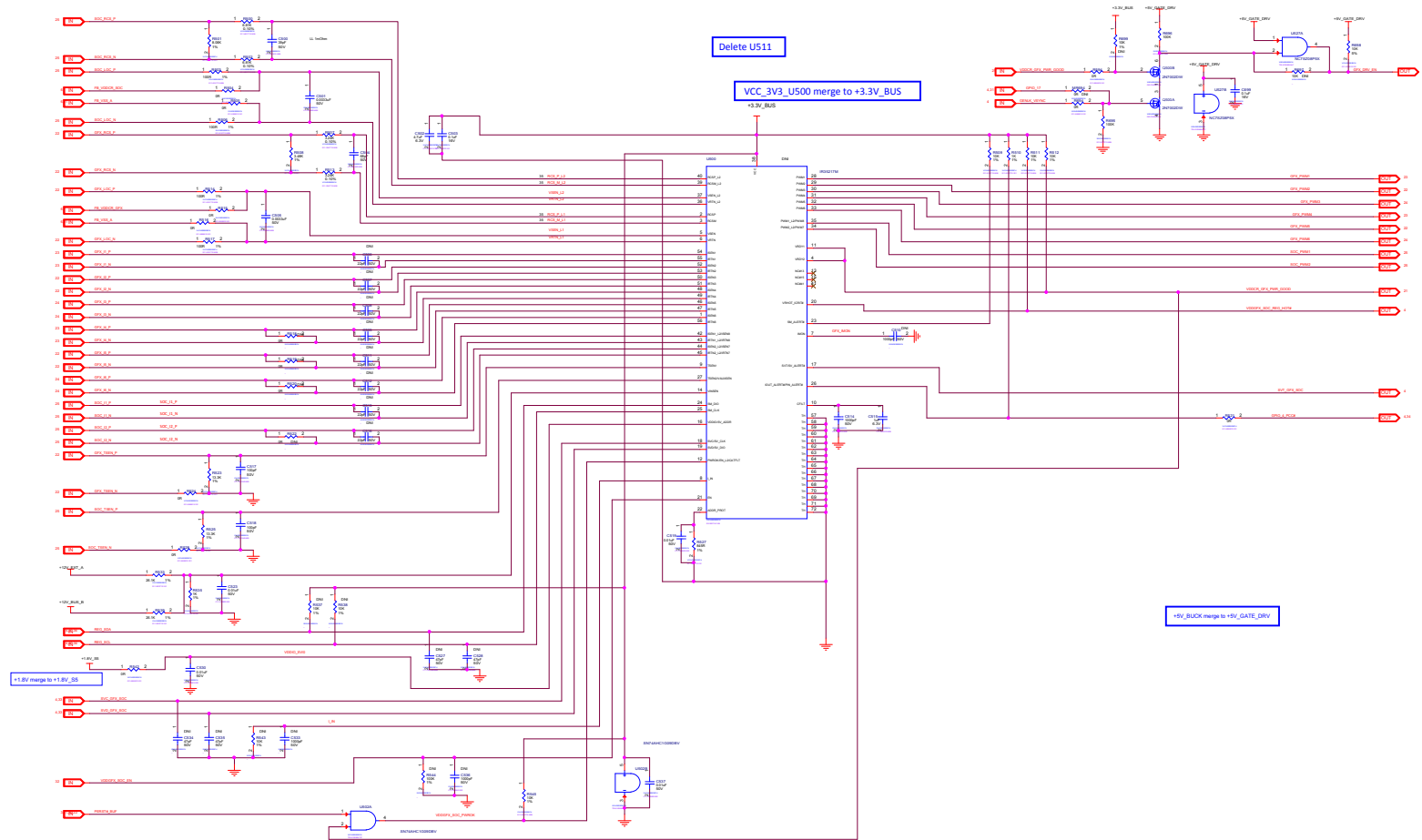
MVDD\_PWR change to +12V\_BUS\_B

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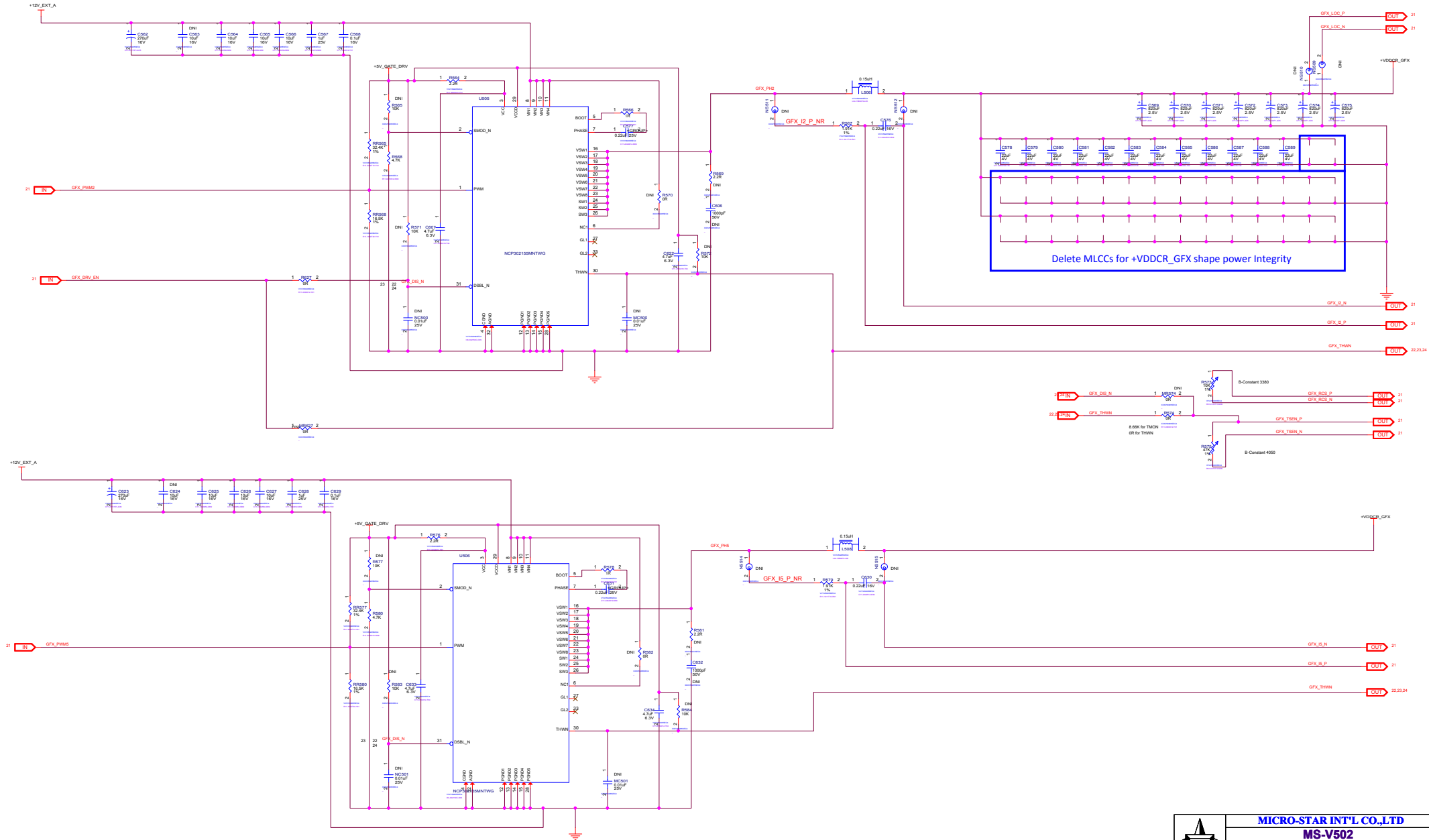
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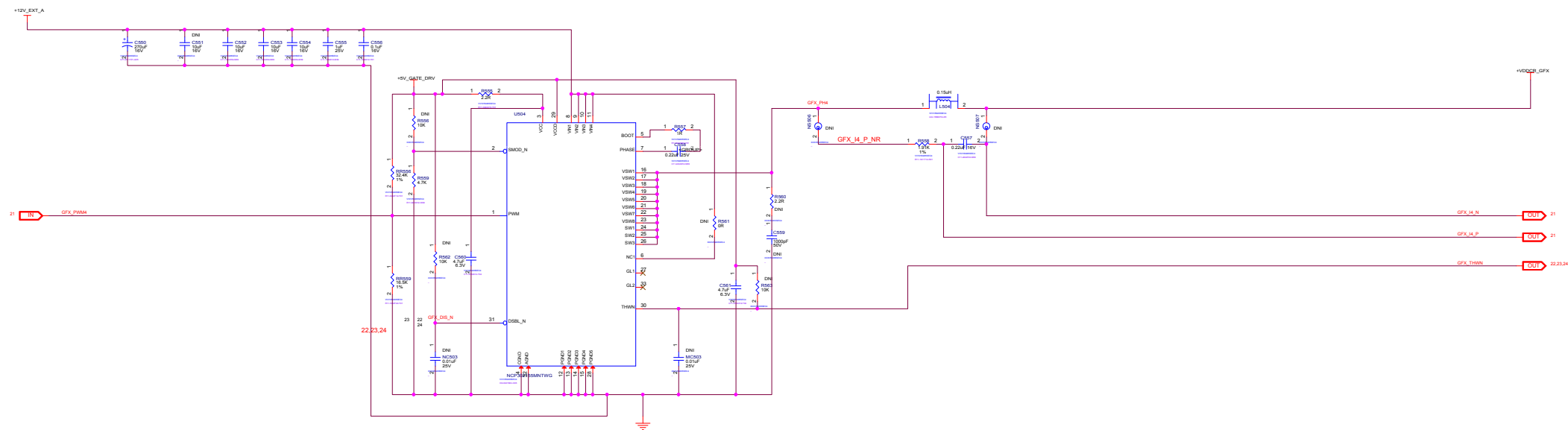
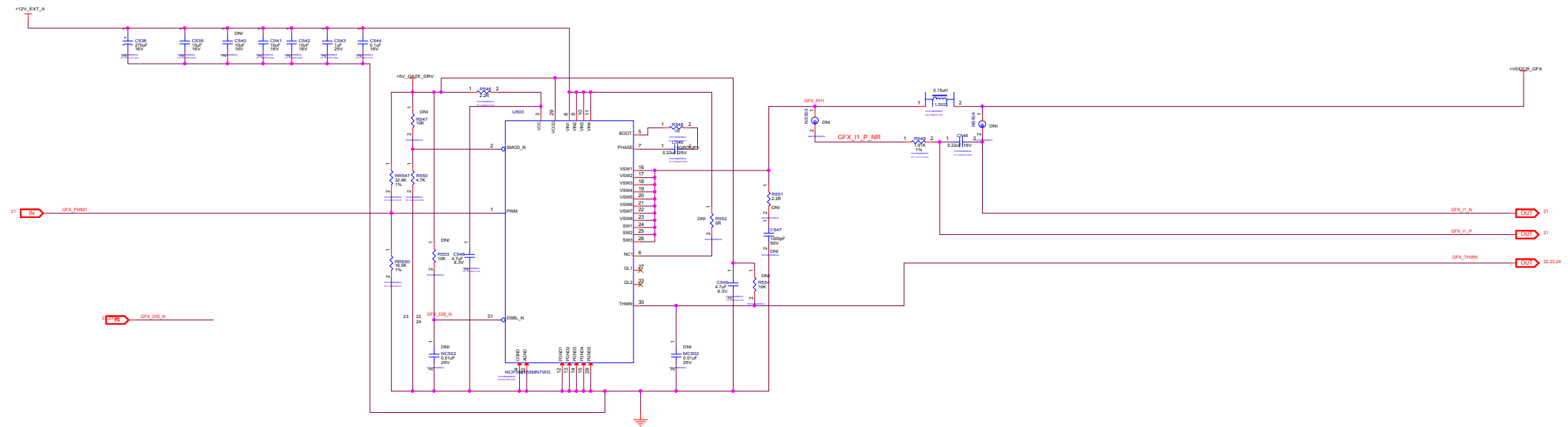
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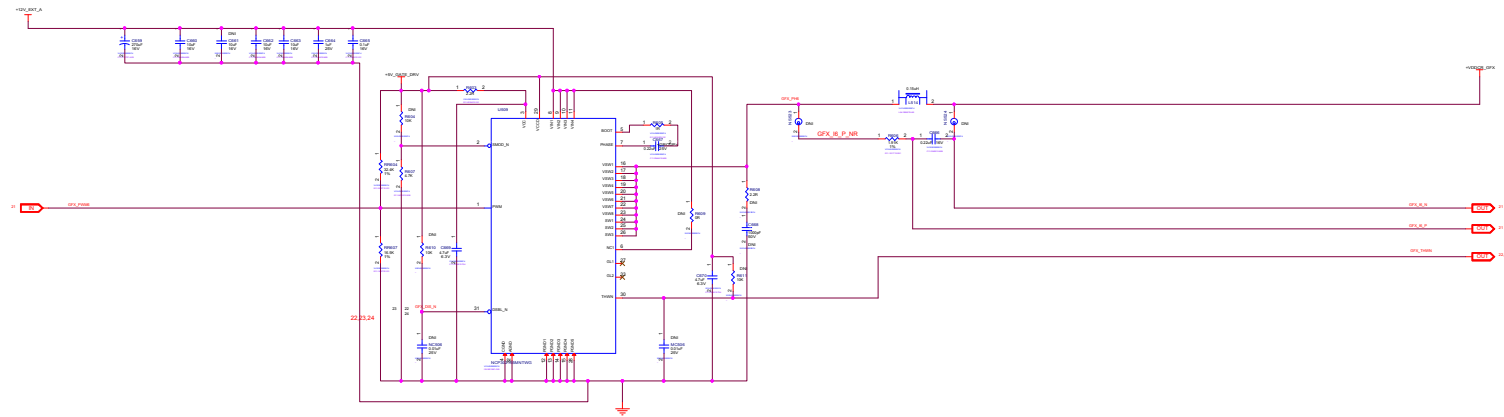




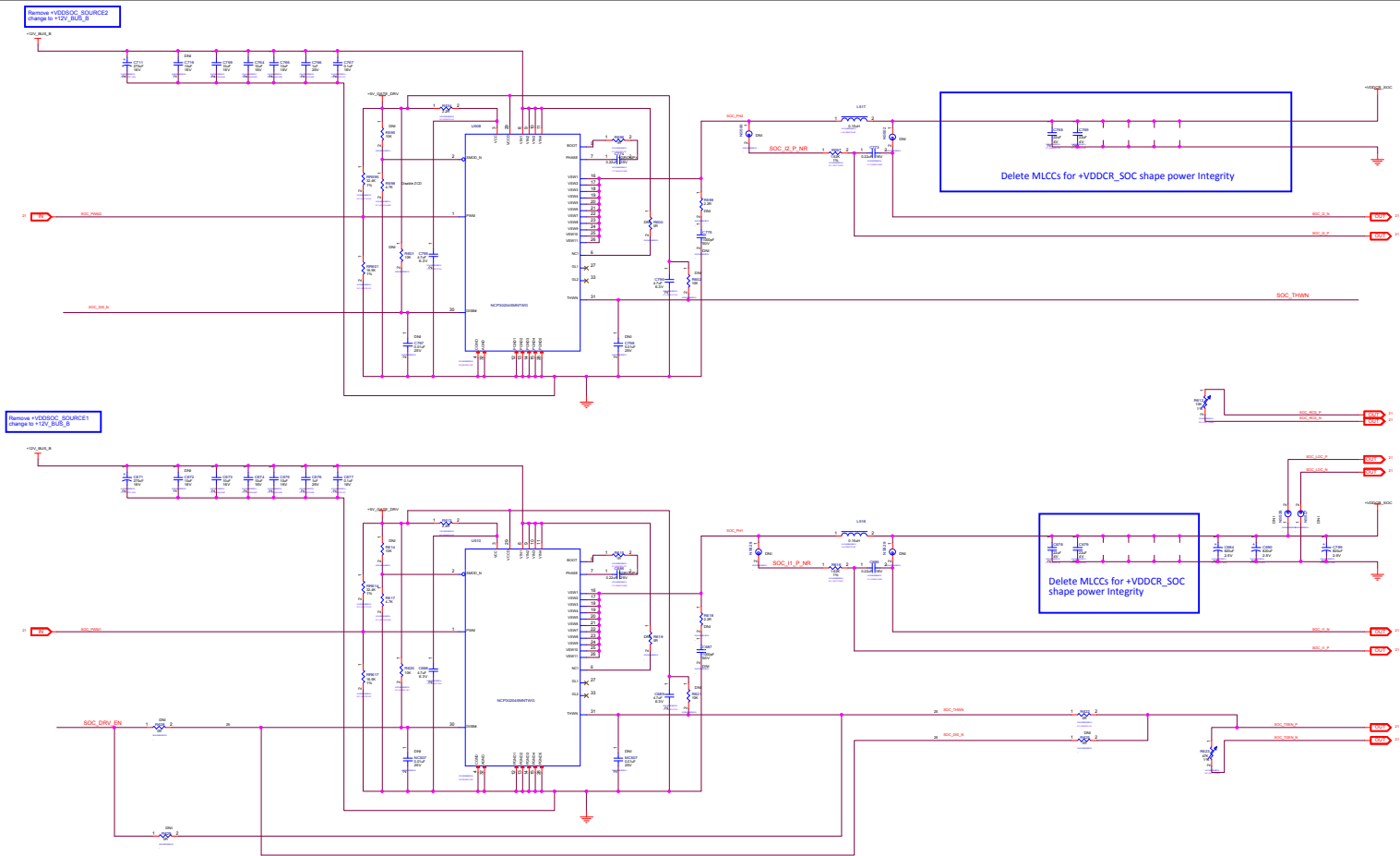
6+2 PHASES : I32-35217HC-I08  
5+1 PHASES : I32-35217JC-I08

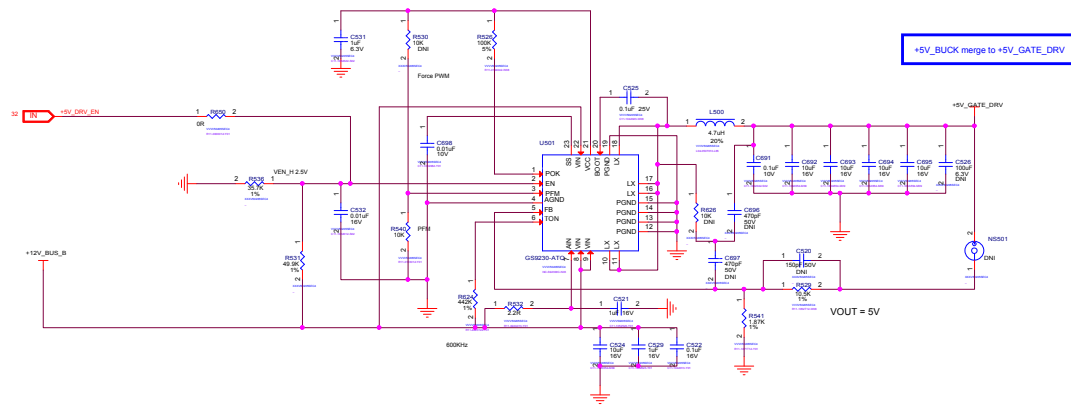


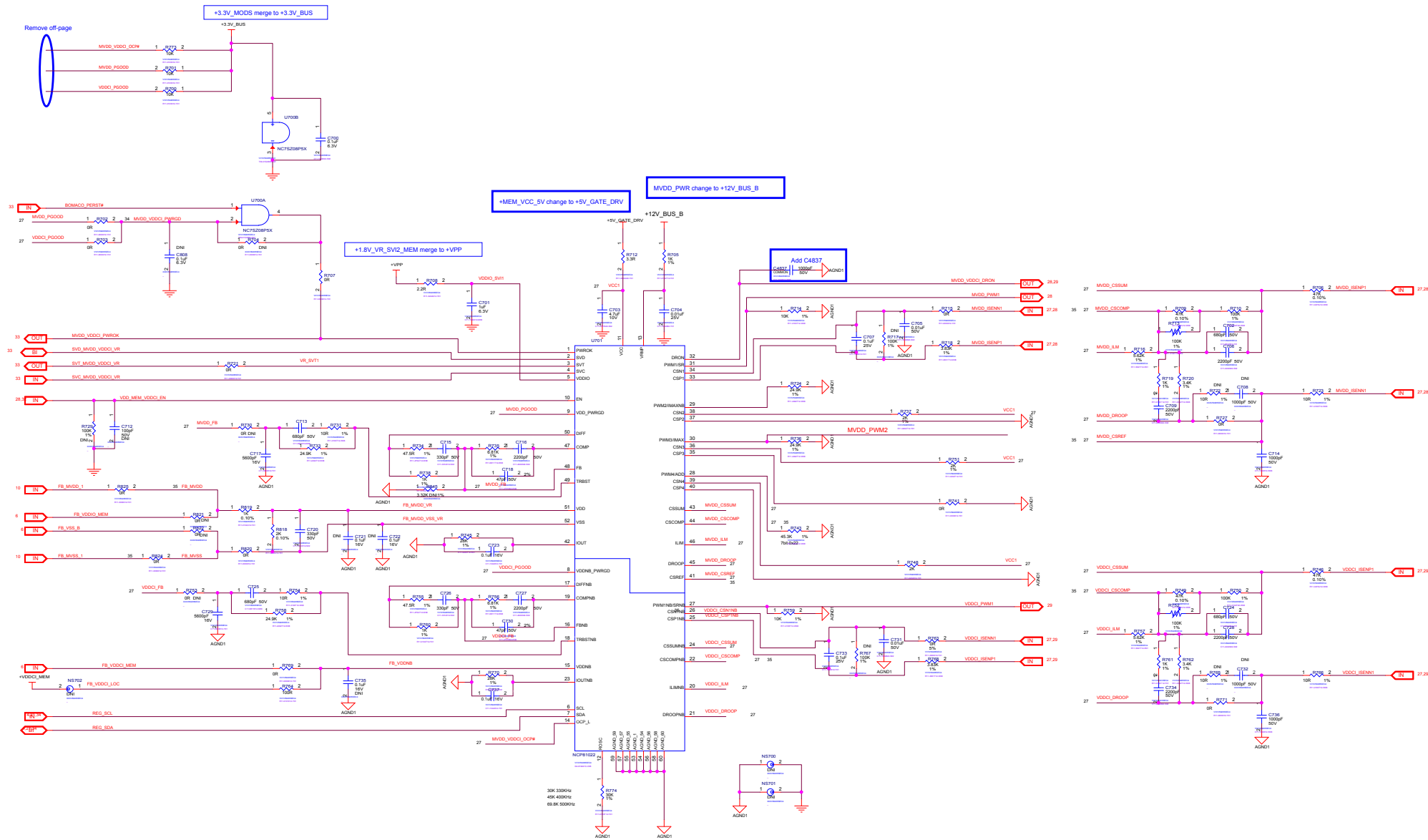






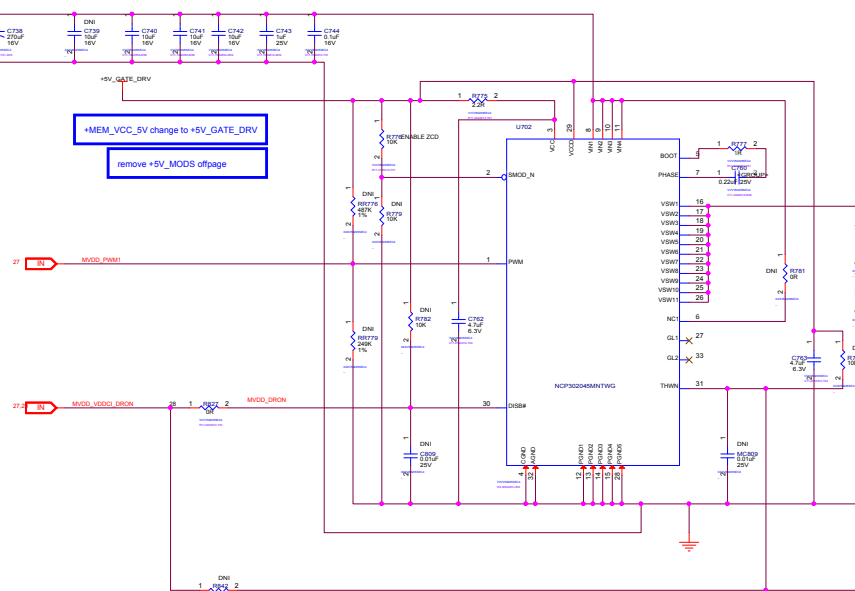




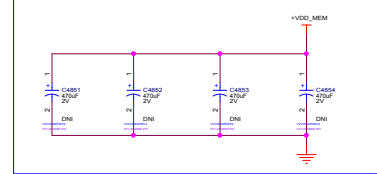


MVDD\_PWR change to +12V\_BUS\_B

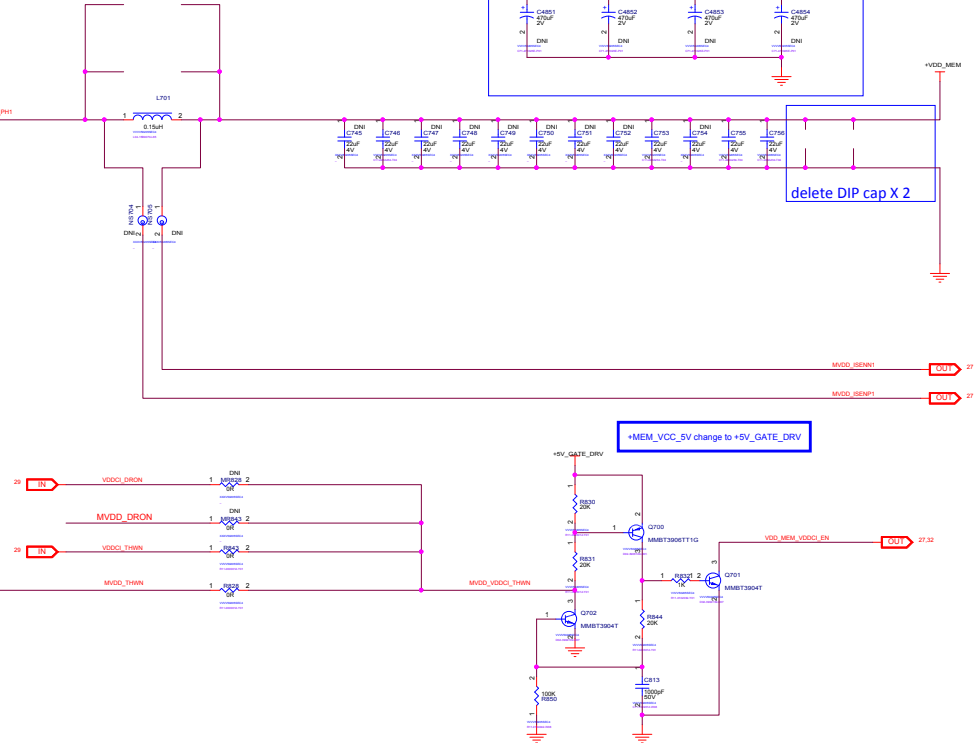
+12V\_BUS\_B

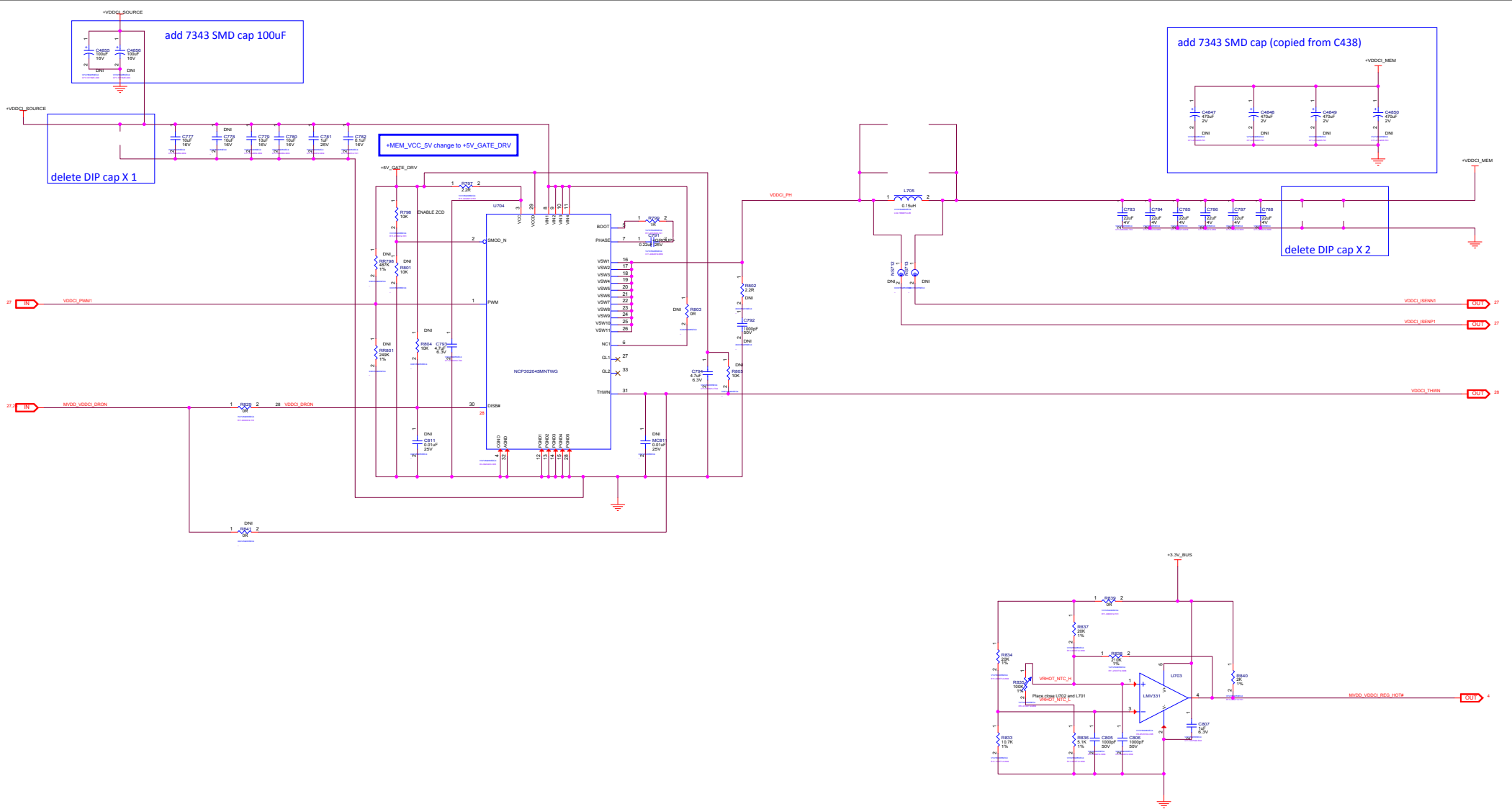


add 7343 SMD cap (copied from C438)

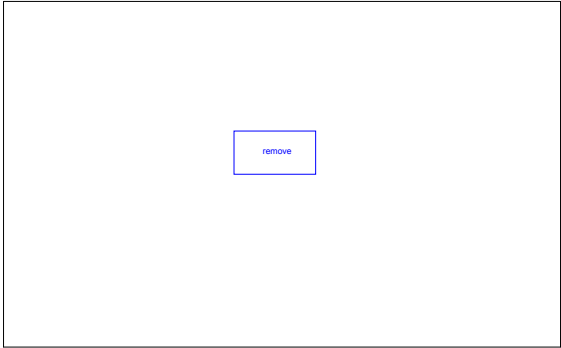


delete DIP cap X 2

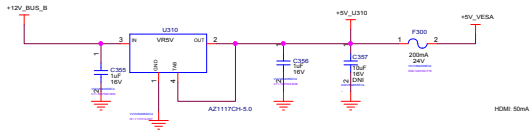


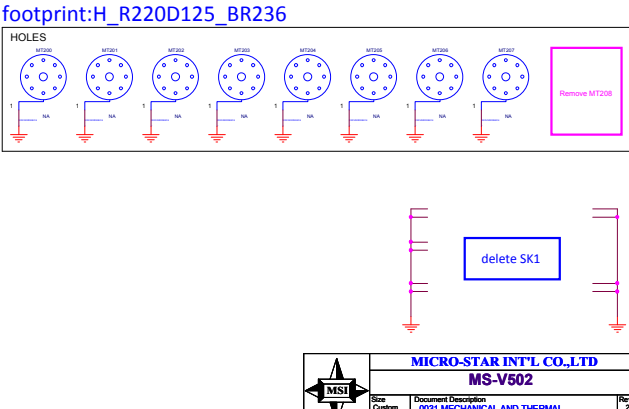
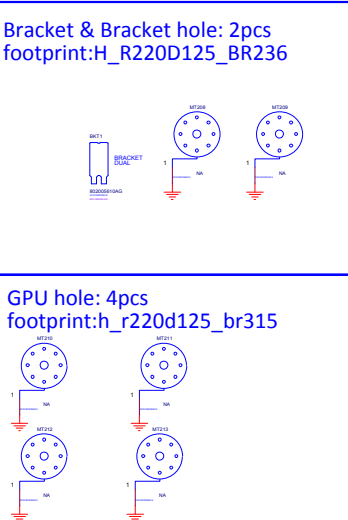
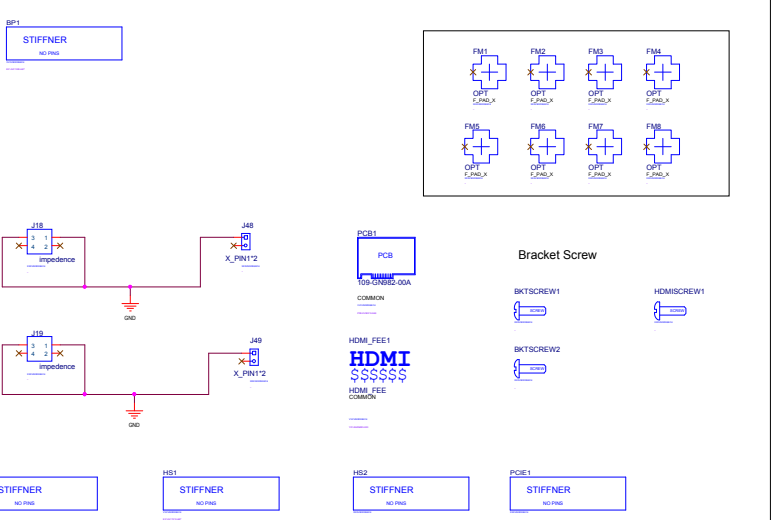
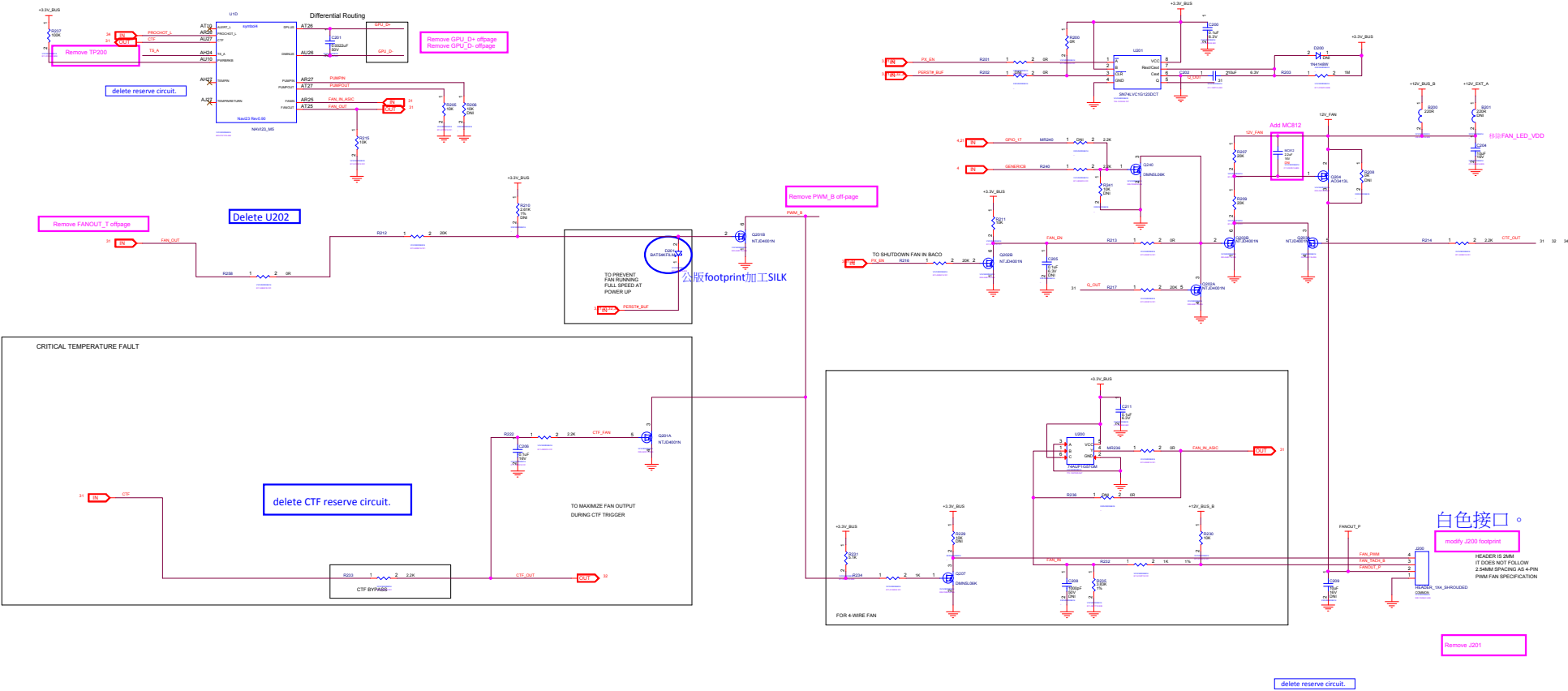


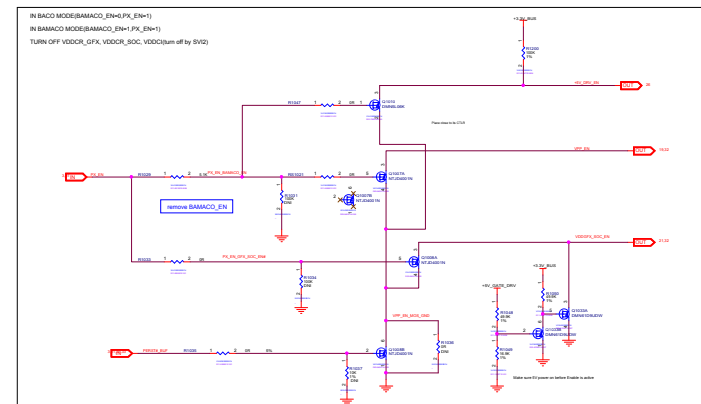
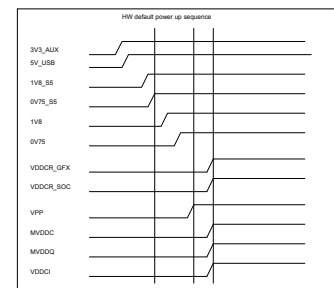
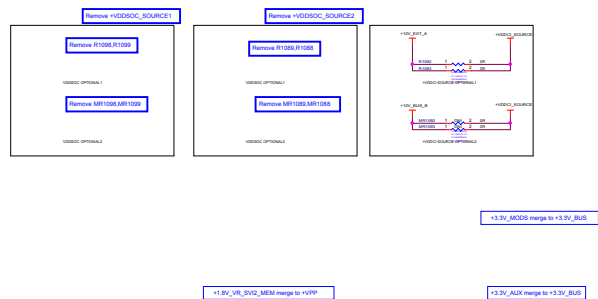
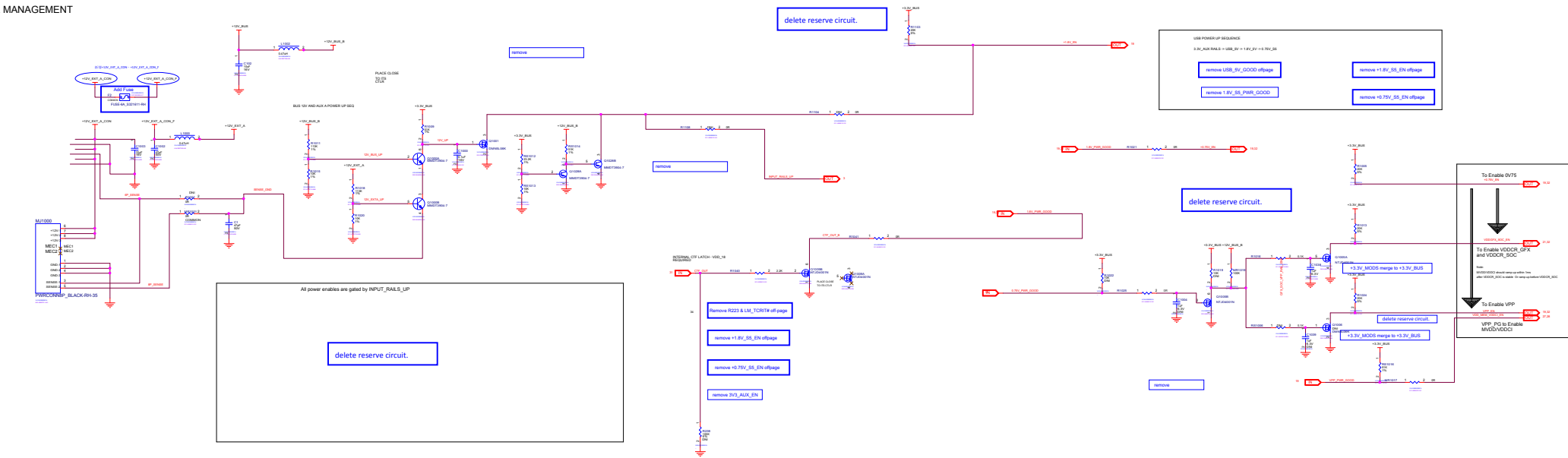
+1.8V FOR BOMACO



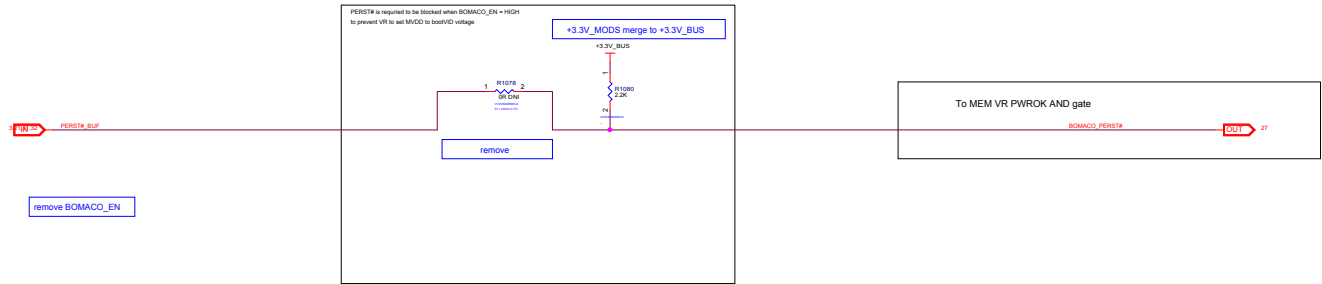
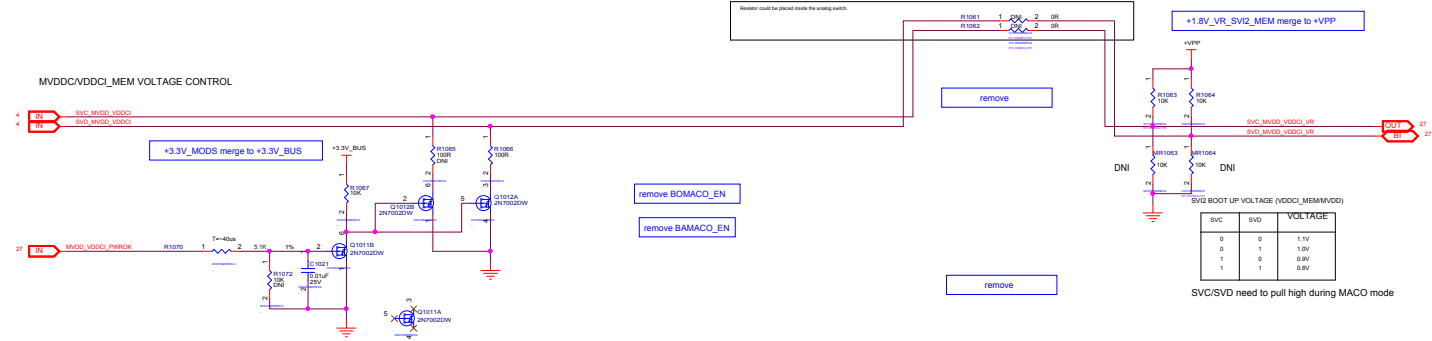
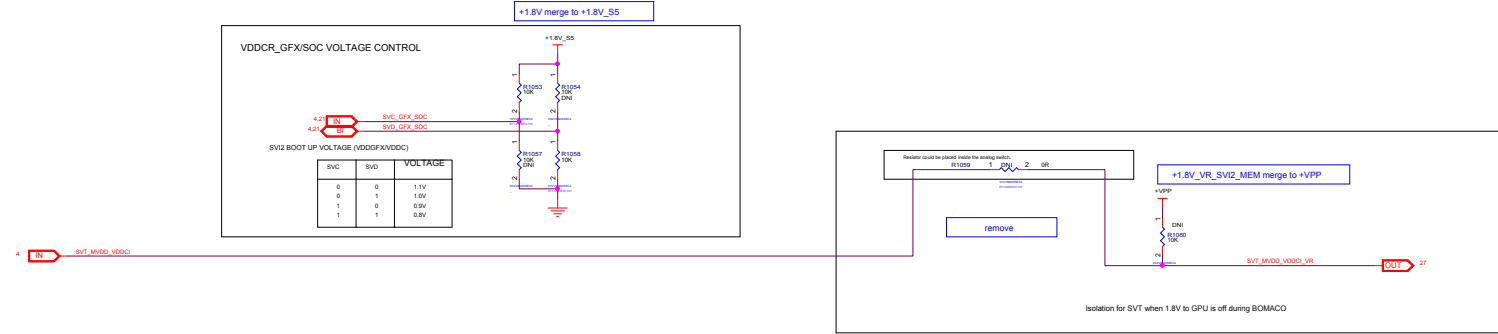
+5V\_VESA FOR HDMI



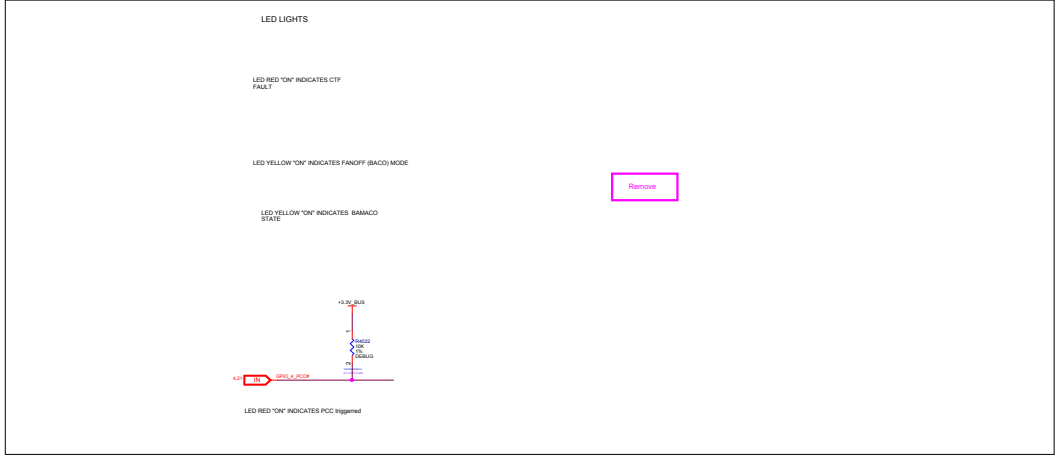
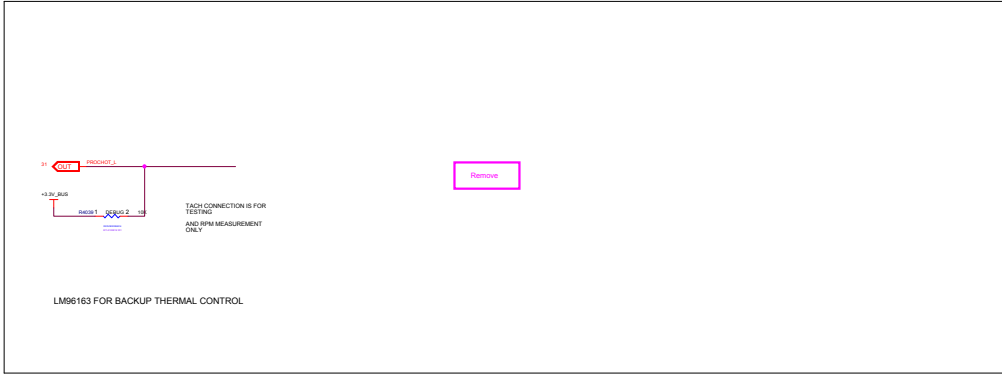
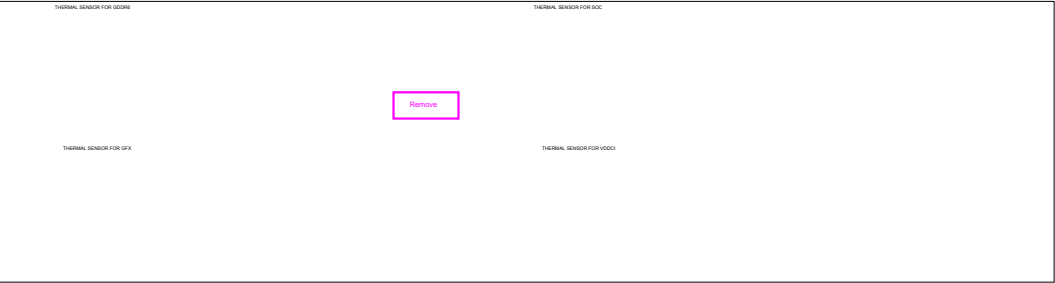
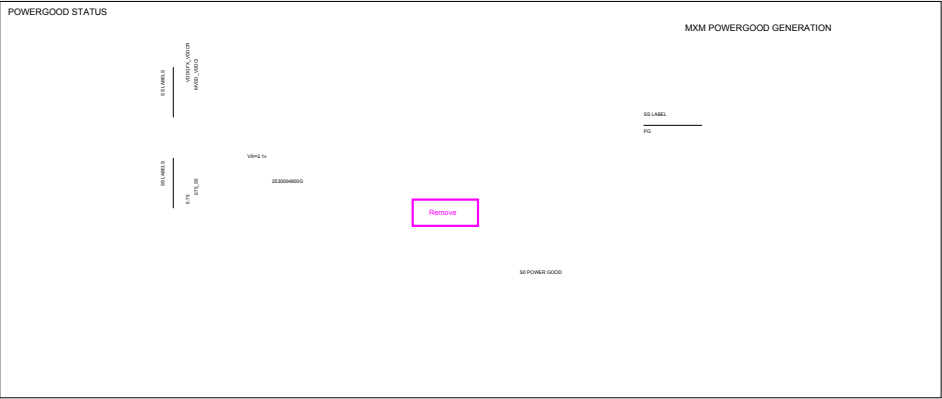
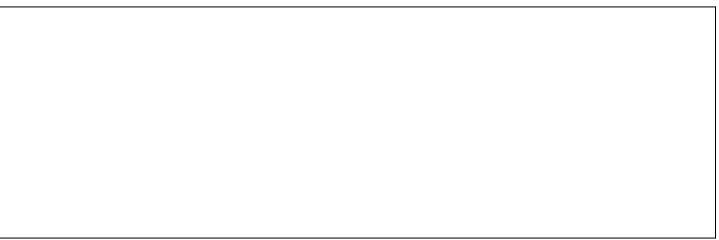
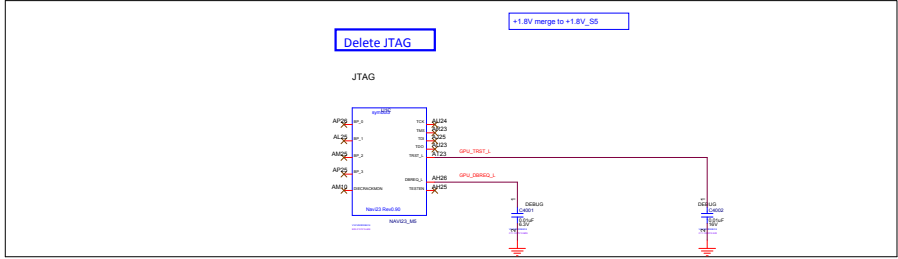








(29) DEBUG CIRCUIT



Remove PI Debug

8

7

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4

3

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AMD



TITLE:

NAVI23 DT XT GDDR6 x16 BOARD

DOCUMENT NUMBER:

105-D532xx-00

DATE:

Tue Jul 07 03:31:54 2020

SHEET NUMBER:

36

 OF 

36

REV:

008

REVISION HISTORY

ENGINEER:

Yahyazadeh, Danial

NOTES:

NOTE

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AMD - PLATFORM HARDWARE ENG  
No.669, HUANKE ROAD  
SHANGHAI, CHINA 201203

SCH Rev	PCB Rev	Date	REVISION DESCRIPTION
00A	00A	20/10/2020	Initial schematic
00B	00B	05/03/2020	Change all ESD based on EMF's new requirement Add Q1033 related circuit for VDDGFX_SOC_EN control to resolve the potential risk on SACO waf(P20)
		07/06/2020	Change +3.3V_MCODR_VSV_MCODR_VSV_GATE_DRV circuit(P20,P21)

MSI

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MS-V502

Size Custom

Document Description 0036 REVISION HISTORY

Date: Wednesday, May 19, 2021

Rev 2.0

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Remove LED\_CONTROLLER\_IT8295